FORM PTO-1082

SEED and BERRY LLP
6300 Columbia Center
Seattle, Washington 98104-7092
Phone (206) 622-4900
Fax (206) 682-6031

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Express Mail Certificate No.: **EM330171687US**
Docket No.: **660073.555**
Date: **May 15, 1997**

BOX PATENT APPLICATION
ASSISTANT COMMISSIONER FOR PATENTS
2011 JEFFERSON DAVIS HIGHWAY
WASHINGTON DC 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventor: **Leland R. Nevill**

For: **METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS**

Enclosed are:

[X] One (1) sheet of drawings (Figs. 1-3).
[X] An assignment of the invention to: Micron Technology, Inc., a corporation of the State of Delaware.
[X] A Declaration and Power of Attorney.
[] A verified statement to establish small entity status under 37 C.F.R. 1.9 and 37 C.F.R. 1.27.
[] A certified copy of Application No. , filed , from which priority is claimed, .
[X] The filing fee has been calculated as shown below.
[] Filed without fee or formal papers.

			Small Entity		or	Other Than A Small Entity	
For:	**No. Filed**	**No. Extra**	**Rate**	**Fee**	**or**	**Rate**	**Fee**
Utility Fee				**$ 385**	**or**		**$ 770**
Total Claims	**18**	**0**	**x 11**	**$**	**or**	**x 22**	**$ 0**
Independent Claims	**4**	**1**	**x 40**	**$**	**or**	**x 80**	**$ 80**
( ) Multiple Dependent Claim Presented			**+ 130**	**$**	**or**	**+ 260**	**$ 0**
ASSIGNMENT			**+ 40**	**$**	**or**	**+ 40**	**$ 40**
			TOTAL	**$**	**or**	**TOTAL**	**$ 890**

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[X] Any additional filing fees required under 37 C.F.R. 1.16.
[X] Any patent application processing fees under 37 C.F.R. 1.17.

Respectfully submitted,
SEED and BERRY LLP

John C. Stewart
Registration No. 40,188

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SEED and BERRY LLP
6300 Columbia Center
Seattle, Washington 98104-7092
Phone (206) 622-4900
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METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS

TECHNICAL FIELD

This invention relates generally to integrated circuits, and more particularly to identification information for integrated circuits.

BACKGROUND OF THE INVENTION

Typically, many identical integrated circuits are constructed on a single wafer of semiconductor material, such as monocrystalline silicon or gallium arsenide. The portion of the wafer occupied by a single one of the integrated circuits is called a die. After completed fabrication of the integrated circuits, a series of tests (known as Probe) is performed in which the function of each die is tested. The test data collected for each die is used in subsequent assembly/packaging steps to ensure that only properly functioning die are packaged as integrated circuit chips.

Following the Probe test, the individual dies are separated from one another, and each properly functioning die is encapsulated (usually in plastic or ceramic) in a package having electric leads to form an integrated circuit chip. Subsequently, a series of testing operations is performed for each of the integrated circuit chips, with test data collected for each of the chips.

In order to properly correlate the various test results with the appropriate die or dies, accurate identification of each of the dies is required, both before and after packaging as an integrated circuit chip. The ability to identify particular dies can also be important following completed manufacture of the integrated circuit chip. For example, when an integrated circuit chip unexpectedly fails during later use, the manufacturer of the chip may wish to identify other potentially failing chips and the users of those chips.

Many of today's integrated circuits provide electronically readable identification information which is programmed into the integrated circuit itself—usually during Probe testing. Also, chip packages usually have an ink or laser-scribed mark which provides some useful information, such as date and country of manufacture, product and package types, speed and other test parameters, and manufacturing lot identification. However, information uniquely identifying the particular integrated circuit within a chip is included only in the electronically readable identification information.

The electronically readable identification information is usually available only during those manufacturing procedures in which the integrated circuit is electrically tested. Also, retrieving the electronically readable identification information is usually done with a relatively sophisticated semiconductor testing apparatus, which necessarily makes physical contact with the integrated circuit chip in order to access the identifying information. There exist a number of manufacturing process steps during which such physical contact does not occur, and hence traceable identification of the individual integrated circuit chips through the various manufacturing processes is quite difficult. Also, once the manufacturer ships the integrated circuit chip to a customer, the unique identification information is not readily available.

SUMMARY OF THE INVENTION

A method of identifying an integrated circuit is provided in which the integrated circuit is both programmed with electronic identification information and marked with a corresponding machine-readable optical identification code. The integrated circuit may be marked with an adhesive label, inscribed with a laser, or marked in any of a variety of suitable ways of displaying machine-readable optical identification codes. The integrated circuit may include a plurality of programmable links which are programmed to store

the electronic identification information, or include any of a variety of suitable adapted circuits for non-volatile data storage.

The method further includes the steps of reading the optical identification code and associating it with the corresponding electronic identification information. A look-up table or other suitable correlating means may be used for performing the association step. Alternatively, the optical identification code may encode exactly the same data values as the electronic identification information.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram depicting an integrated circuit which includes an identification circuit and a machine-readable optical mark.

Figure 2 depicts a semiconductor wafer including a plurality of dies, each of which has a machine-readable optical mark.

Figure 3 depicts a packaged integrated circuit chip which has a machine-readable optical mark.

DETAILED DESCRIPTION OF THE INVENTION

In the following description, certain specific details are set forth in order to provide a thorough understanding of embodiments of the present invention. It will be clear, however, to one skilled in the art that the present invention may be practiced without these details. In other instances, well-known circuits and structures have not been shown in detail in order not to unnecessarily obscure the description of the embodiments of the invention.

Figure 1 depicts an integrated circuit 10, which may be any of a wide variety of integrated circuits fabricated by conventional or newly developed methods. The integrated circuit 10 includes a programmable identification circuit 12 having a bank of programmable links 13, for storing electronic identification information uniquely identifying the integrated circuit. The

identification circuit 12 can be any of a variety of circuits suitable for such purpose, whether currently well known or subsequently developed. The programmable links can be fuses, antifuses, or any of a wide variety of circuit elements suitable for non-volatile data storage, whether currently well known or subsequently developed. The method by which the identification circuit 12 is programmed to store the electronic identification information, as well as the method by which such information is retrieved from the identification circuit, can be any of a wide variety of methods for such purpose, whether currently well known or subsequently developed. For example, U.S. Patent No. 5,301,143 to Ohri et al., which is incorporated herein by reference, describes an example programmable identification circuit 12 and methods for storing/retrieving information to/from same.

The integrated circuit 10 also includes a machine-readable optical identification mark 14. The identification mark 14 may be an adhesive label, a laser-scribed mark, or any of a wide variety of suitable marks. The identification mark 14 displays an optical identification code 15 which corresponds with the electronic identification information stored in the programmable identification circuit 12. The optical identification code 15 can be any of a wide variety of machine-readable optical identification codes, whether currently well known or subsequently developed. The optical identification code 15 can be read by any of a wide variety of methods and with corresponding ones of a wide variety of optical code readers, whether currently well known or subsequently developed. For example, a particular optical identification code and a method and apparatus for reading and decoding the code are described in U.S. Patent No. 5,389,770 to Ackley, which is incorporated herein by reference.

Figure 2 depicts a semiconductor wafer 16 on which a plurality of integrated circuits 10 have been constructed, each on a corresponding one of a plurality of semiconductor dies 18. On each of the dies 18 is a corresponding one of a plurality of the optical identification marks 14A, each having an optical

identification code 15A which corresponds with the electronic identification information stored within the identification circuit 12 (see Figure 1). Figure 3 depicts a packaged integrated circuit chip 20, within which one of the dies 18 (see Figure 2) is encapsulated. The integrated circuit 10 (see Figures 1 and 2) is electrically accessible via a plurality of electric leads 22. An outer surface of the packaged chip 20 is marked with an optical identification mark 14B having an optical identification code 15B which corresponds with the electronic identification information stored within the identification circuit 12 (see Figure 1). Note that distinct reference numerals are used to identify the optical identification marks and codes in Figures 1-3, indicating that various non-identical identification marks and codes may be used at different stages of the manufacturing process.

Typically, the electronic identification information is programmed into the identification circuit 12 during Probe testing of the various dies 18 included in the wafer 16. One or more of the identification marks 14-14B could then be produced to include an optical identification code which encodes data that is identical to the data stored in the identification circuit 12. In other words, the electronically accessible pattern of 1's and 0's stored in the identification circuit 12 is the same as the optically accessible pattern of 1's and 0's encoded in one or more of the identification marks 14-14B. Alternatively, one or more of the identification marks 14-14B can be correlated, via a look-up table or other conventional correlation means, with the particular electronic identification data stored in the identification circuit 12—a more flexible approach than requiring identical data.

Those skilled in the art will appreciate a number of advantages achieved by the above-described embodiments of the present invention. Conventionally, integrated circuits have included only the electronically accessible identification information, as well as visual marking information intended for human eyes. Thus accurate identification of individual integrated

circuits has been available only during manufacturing processes in which the integrated circuit is electrically accessed. In contrast, the present invention provides identification marks having an optical identification code associated with the electronic identification information, thereby providing convenient, accurate and traceable identification of individual integrated circuits during and following the manufacturing process. Also, the ability to optically identify the integrated circuit avoids the need for physical contact, thereby minimizing the possibility of damage to the integrated circuit by the act of electronically reading the identification data—a common concern with current technology.

As stated above, the optical identification marks 14-14B can be any of a wide variety of such marks, and the method and apparatus for encoding optical identification information and reading such information can be any of a wide variety of suitable ones for such purpose. Similarly, the identification circuit 12 can be any of a wide variety of suitably adapted circuits, and the particular methods for programming and retrieving electronic identification information thereto and therefrom can be any of a wide variety of suitably adapted methods. It is the combination of both electrically accessible identification information and associated machine-readable optical identification codes which provides traceability of the integrated circuit through the manufacturing process, as well as after it has been shipped to a customer.

While certain embodiments of the invention have been described for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Numerous variations are well within the scope of this invention, and accordingly, the invention is not limited except by the appended claims.

CLAIMS

1. A method of identifying an integrated circuit, comprising the steps of:

programming the integrated circuit with an electronic identification information; and

marking the integrated circuit with an optical identification code which corresponds with the electronic identification information.

2. The method of claim 1, further comprising the steps of:

reading the optical identification code; and

associating the optical identification code with the corresponding electronic identification information.

3. The method of claim 2 wherein the step of associating the optical identification code with the corresponding electronic identification information includes the step of accessing a look-up table.

4. The method of claim 1 wherein the step of programming the integrated circuit with an electronic identification information includes the step of programming one of a plurality of programmable links.

5. The method of claim 1 wherein the step of marking the integrated circuit with an optical identification code includes the step of placing an adhesive label on the integrated circuit.

6. The method of claim 1 wherein the step of marking the integrated circuit with an optical identification code includes the step of inscribing a symbol on the integrated circuit.

7. In an integrated circuit which includes a programmable circuit for storing an electronically readable identification code which identifies the integrated circuit, a method of identifying the integrated circuit, comprising the steps of:

marking the integrated circuit with an optical identification code; and

associating the optical identification code with the electronically readable identification code.

8. The method of claim 7 wherein the step of associating the optical identification code with the electronically readable identification code includes the steps of:

reading the electronically readable identification code;

reading the optical identification code; and

correlating the read electronically readable identification code with the read optical identification code.

9. The method of claim 8 wherein the step of correlating the read electronically readable identification code with the read optical identification code includes the step of creating a look-up table.

10. The method of claim 7 wherein the step of associating the optical identification code with the electronically readable identification code includes the step of encoding identical data in the optical and electronically readable identification codes.

11. An integrated circuit, comprising:

a programmable identification circuit operable to store identification data; and

an optical identification mark encoding information corresponding to the identification data.

12. The integrated circuit of claim 11 wherein the programmable identification circuit includes a plurality of programmable links.

13. The integrated circuit of claim 11 wherein the optical identification mark encodes information identical to the identification data.

14. An integrated circuit chip, comprising:

a housing;

an integrated circuit enclosed within the housing and including an identification circuit operable to store identification data; and

an optical mark positioned on an exterior surface of the housing and encoding identification information corresponding to the identification data.

15. The integrated circuit chip of claim 14, further comprising electrical contacts connected to said housing and adapted to provide electrical connection between the integrated circuit and circuitry external to the housing.

16. The integrated circuit chip of claim 14 wherein the optical mark is a first optical mark encoding first identification information, and further comprising a second optical mark position on the integrated circuit enclosed within the housing and encoding second identification information corresponding to the identification data.

17. The integrated circuit chip of claim 16 wherein the first identification information is identical to the second identification information.

18. The integrated circuit chip of claim 14 wherein the identification information is the same as the identification data.

METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS

ABSTRACT OF THE DISCLOSURE

An integrated circuit and method for identifying same is described. The integrated circuit includes a programmable identification circuit for storing electronic identification information. The integrated circuit also includes an optical identification mark displaying a machine-readable optical identification code which corresponds with the electronic identification information stored in the identification circuit. The data encoded in the optical identification code may be identical with that of the electronic identification information. Alternatively, a look-up table or other correlating means may be employed to associate the optical identification code with the electronic identification information. The integrated circuit is packaged in a housing, and another optical identification mark is placed on an external surface of the housing. This second optical identification mark displays a machine-readable optical identification code which is identical or correlated to the electronic identification information stored in the identification circuit and/or the optical identification code displayed by the optical identification mark on the integrated circuit. Consequently, convenient and traceable identification of individual integrated circuits is provided during and after manufacture.

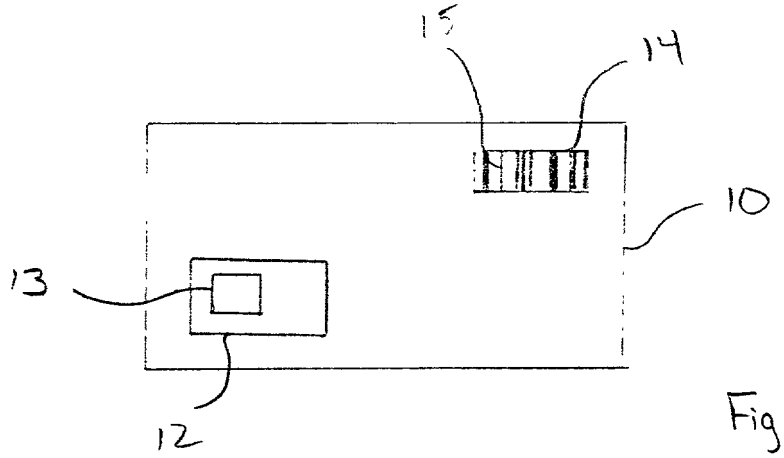

Fig. 1

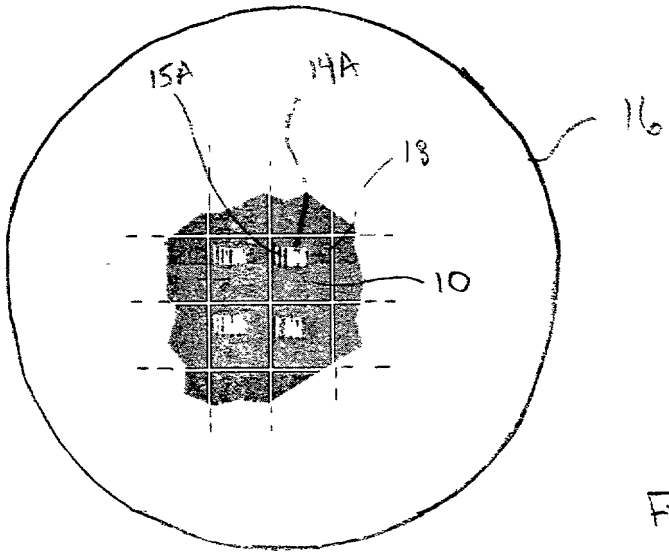

Fig. 2

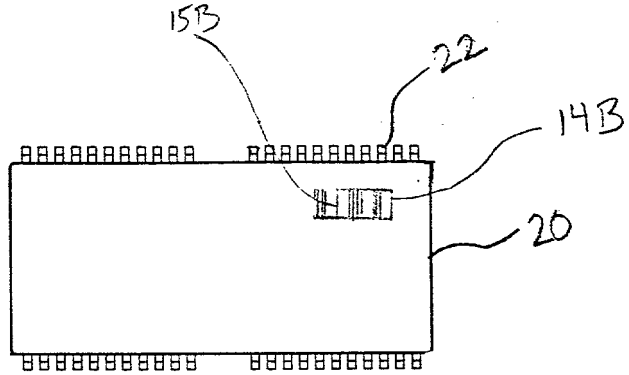

Fig. 3

DECLARATION AND POWER OF ATTORNEY

As the below-named inventor, I declare that:

My residence, post office address, and citizenship are as stated below under my name.

I believe I am the original, first, and sole inventor of the invention entitled "METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS," which is described and claimed in the foregoing specification and for which a patent is sought.

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to herein (if any).

I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application in accordance with 37 C.F.R. § 1.56(a).

I hereby appoint RICHARD W. SEED, Registration No. 16,557; ROBERT J. BAYNHAM, Registration No. 22,846; EDWARD W. BULCHIS, Registration No. 26,847; GEORGE C. RONDEAU, JR., Registration No. 28,893; DAVID H. DEITS, Registration No. 28,066; WILLIAM O. FERRON, JR., Registration No. 30,633; PAUL T. MEIKLEJOHN, Registration No. 26,569; DAVID J. MAKI, Registration No. 31,392; RICHARD G. SHARKEY, Registration No. 32,629; DAVID V. CARLSON, Registration No. 31,153; MAURICE J. PIRIO, Registration No. 33,273; KARL R. HERMANNS, Registration No. 33,507; DAVID D. McMASTERS, Registration No. 33,963; ROBERT IANNUCCI, Registration No. 33,514; JOSHUA KING, Registration No. 35,570; MICHAEL J. DONOHUE, Registration No. 35,859; LORRAINE LINFORD, Registration No. 35,939; KEVIN J. CANNING, Registration No. 35,470; CHRISTOPHER J. DALEY-WATSON, Registration No. 34,807; STEVEN D. LAWRENZ, Registration No. 37,376; ROBERT G. WOOLSTON, Registration No. 37,263; CLARENCE T. TEGREENE, Registration No. 37,951; ELLEN M. BIERMAN, Registration No. 38,079; BRYAN A. SANTARELLI, Registration No. 37,560; MICHAEL L. KIKLIS, Registration No. 38,939; CAROL NOTTENBURG, Registration No. 39,317; CRAIG S. JEPSON, Registration No. 33,517; PAUL T. PARKER, Registration No. 38,264; JOHN C. STEWART, Registration No. 40,188; ROBERT W. BERGSTROM, Registration No. 39,906; DAVID W. PARKER, Registration No. 37,414; ROBERT E. MATES, Registration No. 35,271; and BRIAN G. BODINE, Registration No. P-40,520, comprising the firm of SEED AND BERRY LLP, 6300 Columbia Center, Seattle, Washington 98104-7092, along with W. BRYAN FARNEY, Registration No. 32,651; MICHAEL L. LYNCH, Registration No. 30,871; and LIA M. PAPPAS, Registration No. 34,095, of Micron Technology, Inc., 8000 South Federal Way, Boise, Idaho 83706-9632, as my attorneys to prosecute this application and transact all business in the

Patent and Trademark Office connected therewith. Please direct all telephone calls to John C. Stewart at (206) 622-4900 and telecopies to (206) 682-6031.

Please direct all communications to:

John C. Stewart, Esq.
Seed and Berry LLP
6300 Columbia Tower
701 Fifth Avenue
Seattle, Washington 98104-7092

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

Leland R. Nevill

Date 5/13/97

Residence	:	City of Boise, County of Ada State of Idaho
Citizenship	:	United States of America
P.O. Address	:	6803 Diamond Street, Boise, Idaho 83709

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(660073.660073.555)